REMARKS

Status of the Claims

Claims 1-5 are pending in the present application. Claim 1 is independent.

Claim 1 has been amended. Support can be found at paragraphs [0009], [0011], and [0012] of the specification. Thus, no new matter has been added. Reconsideration of this application, as amended, is respectfully requested.

Issue under 35 U.S.C. § 103(a)

Claims 1-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Davis et al., U.S. Patent No. 6,257,760 (hereinafter "Davis") in view of Akiyama et al. US 6,245,647 (hereinafter "Akiyama") and further in view of Yoon et al., U.S. Publication No. 2003/0077870 (hereinafter "Yoon").

In order to obtain a desired degree of the actual surface temperature of the substrates, the present claims set forth the following requirements:

1. *the resistivity of arbitrary semiconductor substrates at a room temperature is previously measured;*

2. *the relationship between the heating temperature and the temperature of the substrate surface, which depends on different cutting positions of a single crystal is obtained, for each of the arbitrary semiconductor substrates having different resistivities;*

3. *the heating temperature is set and adjusted based on (i) the measured resistivity of the semiconductor substrate to be used and (ii) the above mentioned obtained relationship.*

According to this configuration, the heating temperature indicated, for example, by a thermocouple, and the like, can be adjusted in accordance with the difference of the substrates (the difference in their resistivity at the room temperature), based on the thermal difference to be generated between the heating temperature and the actual surface temperature of the substrates. In this way, the surface temperature of the substrate can be controlled accurately so as to be a desired temperature. Thus, an epitaxial layer having a stable quality can be grown with superior reproducibility, and a semiconductor element having superior characteristics can be stably manufactured (see paragraph [0016] in the specification).

The Examiner has asserted in the Office Action that the configurations defined in claim 1 are mainly taught by Davis, and that the present invention will be arrived at by the combination with Akiyama and, if necessary, Yoon. Applicants respectfully disagree.

The primary reference of Davis disclose a technique to form supperlattice structures. According to Davis in FIG. 3, superlattice structures are deposited at a temperature of less than 25°C, to be annealed and cooled down. Then the resistivity of each of the superlattice structures is measured. This is done in order to create a resistivity versus temperature calibration curve. Subsequently, another superlattice structure is subjected to heat processing in a processing chamber to measure the resistivity and thus, the process temperature is determined by using the calibration curve. Applicants note that what is annealed in Davis is not the bare substrate of silicon but rather the superlattice structure.

In comparing the techniques disclosed in Davis and the present invention, Applicants wish to clarify that what is subjected to the resistivity measurement and the temperature control is the superlattice structure in Davis, whereas it is the semiconductor substrate (e.g., InP bare substrate) in the present invention. Thus, there is nothing in common with regard to the property and behavior between the superlattice structure of Davis and the semiconductor substrate of the present invention. The reason is that a substance with superlattice structure is composed in a state where phases of sublattices of distinctly different alternating layers are deposited, whereas a semiconductor substrate comprises an even bulk single crystal material. Accordingly, a substance with superlattice structures and a semiconductor substrate would show great differences in their property when being heated. Further, a substance with superlattice structure would not show much variation in surface temperature depending on the cutting position of a substrate. In addition, the layers constituting the superlattice structure are deposited in a room temperature and then are annealed in Davis, whereas epitaxial growth is performed in a state where the substrate is being heated in the present invention, which shows significant differences in the manufacturing method as to when the heating step is performed.

As mentioned above, since there is nothing in common with regard to the property and behavior between the superlattice structure of Davis and the semiconductor substrate of the present invention, and because of the technical gap between the prior art from the present invention, one skilled in the art cannot have been motivated to apply the disclosure of Davis to a vapor phase growth method to arrive at the present invention.

Further, the Examiner admits that the primary reference fails to teach a vapor phase growth method, but relies upon Akiyama stating that the reference discloses a method for forming a thin film uniform in resistivity distribution on a semiconductor substrate. In response, Applicants note the following:

Akiyama pertains to a technique to supply trichlorosilane ($SiHCl_3$) gas and diborane (B_2H_6) gas on a silicon semiconductor single crystal substrate and to form a silicon semiconductor single crystal thin film having a predetermined resistivity. The disclosure is characterized in that the thin film is formed in a state where the temperature of the inside-wall of the reaction vessel of vapor phase growth equipment is controlled to be below the thermal decomposition temperature of diborane, for example, to within a range of room temperature to 250°C. Akiyama also mentions in Example 1 forming the silicon single crystal thin film by increasing the temperature of the substrate to 1000°C, and controlling the inside-wall temperature of the reaction vessel to below 250°C. Here, Akiyama merely discloses controlling the inside-wall temperature of the reaction vessel in order to adjust the thermal decomposition temperature of diborane. However, Akiyama does not disclose any indication for an accurate temperature control under the conditions defined by claim 1. Accordingly, Akiyama does not provide any suggestion to arrive at the present invention.

In addition, Yoon discloses a method to reduce parasitic capacitance in an InP/InGaAs DHBT by selective wet etching. However, Yoon does not disclose any details regarding a vapor phase growth method, much less any indication for accurate temperature control. Accordingly, Yoon does not provide any suggestion or motivation to modify Davis or Akiyama.

On the other hand, the present invention provides a method to obtain the appropriate substrate temperature based upon its own resistivity that the substrate to be subjected to the heating process originally has.

None of Davis, Akiyama, Yoon, or the combination thereof suggests the variation in surface temperature to be generated in heating process, deriving from the resistivity difference that the substrate originally has, thereby the temperature control cannot be performed with reproducibility and with perfection as in the present invention.

In view of the foregoing, since the configurations defined in the vapor phase growth method as claimed are not at all taught by the combination of the cited references, even if the references were combinable in the manner suggested by the Examiner, such combination still

fails to achieve or render obvious the above described features as defined in amended claim 1, and advantageous effects obtained therefrom.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Craig A. McRobbie, Registration No. 42874 at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

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Respectfully submitted,

By _____ #42,874

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